REMARKS

As a preliminary mater, Applicant appreciates the Examiner's indication of allowable subject matter contained in claims 4-10 if the §112, second paragraph, rejection of these claims is overcome.

As a further preliminary matter, the title of the invention is amended to "Method for Fabricating a Thin Film Transistor Using a Half-Tone Mask," as suggested by the Examiner. For this reason, withdrawal of the objection to the title is respectfully requested.

Claims 2-10 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite. More specifically, the Examiner objects to the claim language "to be formed" in the claim. Accordingly, Applicant amended the claim language to delete the "to be" claim language and requests withdrawal of the §112 rejection of claims 2-10 on this basis.

Claims 1-3 stand rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al. (U.S. Patent No. 6,468,840). In response, Applicant amended independent claims 1-3, and requests withdrawal of the §102(b) rejection based on these amendments. Claims 1-2 now more clearly define that the resist in a channel formed area is thinner than the resist in areas other than the channel formed area within the thin film transistor area. Claim 3 now clarifies that the resist pattern is formed such that the film thickness of the resist in the gate bus-line formed area is thicker than the resist in the pixel electrode formed area.

Tanaka discloses in column 11, lines 30-45 and shows in FIGs. 15(a)-(e) that a second photo resist 108 is formed thicker than a photo resist in another area. For example, Tanaka shows the second photo resist 108 as being thicker than the photo resist in areas of the pixel electrode 209, the gate terminal portion 210, and the drain terminal portion 211, which are formed from the ITO film 107.

Furthermore, Tanaka has a film thickness of the resist in a gate bus-line formed area that is the same thickness as the film thickness of the resist in the pixel electrode formed area. Tanaka fails to disclose or suggest formation of the channel area by forming a resist in a channel formed area thinner than the resist in the other areas, as recited in amended claims 1-2, or that a resist in a gate bus-line formed area has a thickness greater than that of a pixel electrode formed area, as recited in amended claim 3.

In contrast, amended claims 1-2 of the present application now define the resist in a channel formed area as being thinner than the resist in areas other than the channel formed area within the thin film transistor formed area. Claim 3 is also amended to clarify that the resist pattern is formed such that the film thickness of the resist in the gate bus-line formed area is thicker than the resist in the pixel electrode formed area. Accordingly, in the present application, a resist does not need to be formed for formation of a gate bus-line area. Advantageously, the present invention provides a simpler way to form a gate bus-line area. Since Tanaka fails to disclose or suggest the above-recited

features, and cannot simplify the formation of the gate bus-line area like the present application, withdrawal of the §102(b) rejection of claims 1-3 is respectfully requested.

For all of the foregoing reasons, Applicant submits that this Application is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 
Joseph P. Fox
Registration No. 41,760

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300 South Wacker Drive
Suite 2500
Chicago, Illinois 60606
(312) 360-0080
Customer No. 24978